What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method of sensing a stored value of a programmable conductor random access memory element, the method comprising:

precharging a digit line and a digit complement line to a predetermined voltage value;

activating an access transistor coupled between said element and said digit line to apply a read voltage to said element; and

comparing the voltage on said digit line with a voltage on said digit complement line to determine a logical state of said element.

2. The method of claim 1, wherein said act of precharging comprises precharging said digit line and said digit complement line to approximately Vdd.

3. The method of claim 1, wherein said act of precharging comprises receiving a precharge control signal at a precharge circuit and coupling said digit line and said digit complement line to approximately Vdd.

4. The method of claim 1, wherein said act of precharging further comprises equilibrating said voltage on said digit line and said voltage on said digit complement line.

5. The method of claim 1, wherein said act of activating comprises firing a rowline coupled to a gate of said access transistor.

6. The method of claim 1 further comprising discharging said voltage on said digit line for a predetermined period of time before said act of comparing.

7. The method of claim 6, wherein said act of discharging further comprises discharging said voltage on said digit line from a voltage value approximately equal to said predetermined voltage plus an additional voltage.

8. The method of claim 7, wherein said additional voltage is due to parasitic capacitance between said digit line and a rowline coupled to said access transistor.

9. The method of claim 1 further comprising reading a low resistance level at said element.

10. The method of claim 9 further comprising rewriting said low resistance level into said element.

11. The method of claim 1 further comprising reading a high resistance level at said element.

12. The method of claim 1 further comprising applying a voltage to a second terminal of said memory element, said voltage being between 0v and said predetermined voltage.

13. The method of claim 12, wherein said act of applying comprises applying said voltage to a cell plate ties to said second terminal of said memory element.

14. A method for reading a semiconductor memory cell, the method comprising:

setting a voltage of a cell plate of said cell, to which a first portion of a resistive element of said cell is coupled, to a first predetermined voltage;

charging a first terminal of an access transistor of said cell and a reference conductor to a second predetermined voltage, wherein said first terminal is coupled to a column line of said cell, wherein a second terminal of said transistor is coupled to a second portion of said resistive element, and wherein said first terminal and said reference conductor are coupled to respective inputs of a comparator;

charging a gate of said access transistor to a third predetermined voltage in order to read said cell, wherein said gate is coupled to a rowline of said cell;

discharging said first terminal from said second predetermined voltage through the resistive element; and

comparing a voltage at said first terminal with said second predetermined voltage a predetermined period of time after said act of discharging begins in order to determine a logical state of said cell.

15. The method of claim 14, wherein said second predetermined voltage is greater than said first predetermined voltage.

16. The method of claim 14, wherein said act of discharging comprises discharging said first terminal from a fourth predetermined voltage that is slightly different from said second predetermined voltage, said fourth predetermined voltage resulting from a parasitic capacitance associated with said column line.

17. The method of claim 14 further comprising changing said third predetermined voltage to a level sufficient to rewrite said resistance level to said memory cell after said memory cell has been read.

18. The method of claim 17, wherein said act of changing comprises increasing said third predetermined voltage to said second predetermined voltage.

19. The method of claim 18, wherein said act of increasing comprises increasing said third predetermined voltage level to approximately Vdd.

20. The method of claim 17 further comprising rewriting said high resistance level to said memory cell.

21. The method of claim 14, wherein said act of setting comprises setting said voltage of said cell plate to approximately Vdd.

22. The method of claim 21, wherein said act of setting comprises setting said voltage of said cell plate to approximately Vdd/2.

23. The method of claim 14, wherein said act of charging a first terminal of a transistor comprises charging said first terminal and said reference conductor to approximately Vdd.

24. The method of claim 14, wherein said act of charging a gate comprises charging said gate to a value sufficient for reading said resistive element, but less than a value that would enable said cell to be programmed.

25. The method of claim 24, wherein said act of charging said gate comprises charging said gate to a voltage level between said first and second predetermined voltages.

26. The method of claim 16, wherein said act of discharging said first terminal comprises discharging said first terminal from approximately Vdd plus an additional voltage.

27. The method of claim 26, wherein said act of discharging said first terminal comprises discharging said first terminal from approximately Vdd plus approximately 0.1V.

28. The method of claim 14, wherein said act of comparing comprises comparing said voltage at said first terminal with said second predetermined voltage approximately 15-30ns after said act of discharging has begun.

29. The method of claim 14 further comprising determining said memory cell has a logic HIGH state.

30. The method of claim 14 further comprising determining said memory cell has a logic LOW state.

31. A method for sensing a stored value of a programmable conductor random assess memory cell, the method comprising:

precharging a digit line coupled to a first terminal of an access transistor of said cell to a first predetermined voltage;

charging a cell plate of said cell to a second predetermined voltage, said second predetermined voltage being a value between 0V and said first predetermined voltage; and

applying a third predetermined voltage to a rowline coupled to a gate of said access transistor such that a resulting voltage across said programmable conductor memory cell is sufficient to read a logical state of said cell, but insufficient to program said cell.

32. A method for sensing a stored value of a programmable conductor random access memory cell, the method comprising:

precharging a digit line to a reference voltage value, said digit line being coupled to a first terminal of an access transistor of said cell;

charging a cell plate of said cell to a first predetermined voltage, said first predetermined voltage being a value between 0V and said reference voltage value;

firing a rowline of said memory cell by applying a second predetermined voltage, said second predetermined voltage being sufficient to read said memory cell, but insufficient to program said memory cell; and

comparing a voltage read at said digit line with said reference voltage in order to determine a logical state of said memory cell.

33. A semiconductor memory structure comprising:

a digit line and a digit complement line;

a circuit for precharging said digit line and said digit complement line to a predetermined voltage value prior to a read operation;

an access transistor for coupling a programmable conductor memory element to said digit line during a read operation; and

a sense amplifier for comparing voltages on said digit line and said digit complement line during said read operation to determine a logical state of said memory element.

34. The structure of claim 33, wherein said predetermined voltage is approximately Vdd.

35. The structure of claim 33, wherein said programmable conductor memory element comprises a chalcogenide glass having first and second electrodes.

36. The structure of claim 35, wherein said chalcogenide glass has a Ge, Se and Ag composition.

37. The structure of claim 33 further comprising a variable parasitic capacitance between said digit line and a rowline of said memory structure, said variable parasitic

capacitance causing said digit line to be charged to a voltage level higher than said predetermined voltage during said read operation.

38. The structure of claim 33, wherein said digit complement line is associated with a memory array different from a memory array with which said memory cell is associated.

39. The structure of claim 33 further comprising an equilibrate circuit for equilibrating said digit line and said digit complement line to said predetermined voltage.

40. A semiconductor memory comprising:

a programmable conductor memory element;

a column line;

a rowline;

a conductor for applying a first voltage to a first terminal of said programmable conductor memory element;

a transistor for selectively coupling said column line to another terminal of said programmable conductor memory element in response to a gate voltage applied to said rowline;

a sense amplifier coupled to said column line and a reference conductor; and

a precharge circuit for precharging said column line and reference conductor to a predetermined voltage prior to application of a gate voltage to said rowline,

said sense amplifier comparing a voltage on said column line and reference line to determine a resistance value of said programmable conductor memory element after said gate voltage is applied to said rowline.

41. The memory of claim 40, wherein said first voltage is a voltage between 0V and approximately Vdd.

42. The memory of claim 40, wherein said programmable conductor memory element comprises a chalcogenide glass having first and second electrodes.

43. The memory of claim 42, wherein said chalcogenide glass has a Ge, Se and Ag composition.

44. The memory of claim 40, wherein said gate voltage is sufficient to read said memory element but insufficient to program said memory element.

45. The memory of claim 40 further comprising a variable parasitic capacitance associated with said column line, said variable parasitic capacitance causing said column line to be charged to a voltage level higher than said predetermined voltage supplied by said precharge circuit in response to said gate voltage being applied to said rowline.

46. The memory of claim 45, wherein said variable parasitic capacitance causes said column line to be charged to approximately 0.1V higher than said predetermined voltage supplied by said precharge circuit.

47. The memory of claim 40, wherein said sense amplifier comprises:

an N-sense amplifier; and

a P-sense amplifier coupled to said N-sense amplifier, wherein said N-sense amplifier and said P-sense amplifier compare voltage values at said column line and said reference conductor.

48. The memory of claim 40, wherein said reference conductor is associated with a memory array different from a memory array with which said memory element is associated.

49. The memory of claim 40 further comprising a dummy rowline associated with said reference conductor, said dummy rowline normally being fired to a dummy rowline voltage and when said gate voltage is applied to said rowline, said dummy rowline is deactivated such that said predetermined voltage at said reference conductor decreases due to parasitic capacitance at a column line associated with said dummy rowline.

50. A processor system, comprising:

a processor; and

a semiconductor memory structure coupled to said processor, said semiconductor memory structure comprising:

a digit line and a digit complement line;

a circuit for precharging said digit line and said digit complement line to a predetermined voltage value prior to a read operation;

an access transistor for coupling a programmable conductor memory element to said digit line during a read operation; and

a sense amplifier for comparing voltages on said digit line and said digit complement line during said read operation to determine a logical state of said memory element.

51. The system of claim 50, wherein said predetermined voltage is approximately Vdd.

52. The system of claim 50, wherein said programmable conductor memory element comprises a chalcogenide glass having first and second electrodes.

53. The system of claim 52, wherein said chalcogenide glass has a Ge, Se and Ag composition.

54. The system of claim 50 further comprising a variable parasitic capacitance between said digit line and a rowline of said memory cell, said variable parasitic capacitance causing said digit line to be charged to a voltage level higher than said predetermined voltage during said read operation.

55. The system of claim 50 wherein said digit complement line is associated with a memory array different from a memory array with which said memory cell is associated.

56. A processor system comprising:

a processor; and

a semiconductor memory coupled to said processor, said semiconductor memory comprising:

a programmable conductor memory element;

a column line;

a rowline;

a conductor for applying a first voltage to a first terminal of said programmable conductor memory element;

a transistor for selectively coupling said column line to another terminal of said programmable conductor memory element in response to a gate voltage applied to said rowline;

a sense amplifier coupled to said column line and a reference conductor; and

a precharge circuit for precharging said column line and reference conductor to a predetermined voltage prior to application of a gate voltage to said rowline,

said sense amplifier comparing a voltage on said column line and reference line to determine a resistance value of said programmable conductor memory element after said gate voltage is applied to said rowline.